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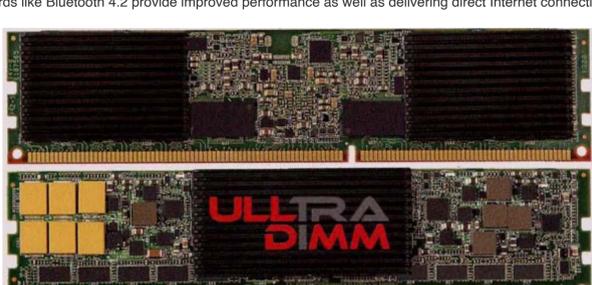
Nonvolatile Storage and 64-bit Arm Cores

Digital Forecast

Digital technology will take some major steps forward this year with technologies like wearable technology, storage, and cloud computing leading the way

THIS LOOKS TO BE A GOOD YEAR for digital technology across the board, from memory to compute. Conventional uses from PCs to smartphones continue to push price and performance, but the growing Internet of Things (IoT) trend is being fed by advances in sensors and low power operation.

Wearable technology is one subset of IoT that will see massive growth (see "What Tech Will You Be Wearing Next Year?" on [electronicdesign.com](#)). It will also place a strain on designers to keep things small, highly functional, and communicating with the rest of the world. Emerging standards like Bluetooth 4.2 provide improved performance as well as delivering direct Internet connectivity.



1. SanDisk UltraDIMM (top/rear, bottom/front) plugs into a standard DDR DIMM socket but it contains flash memory. It can be updated at the row level instead of the block level required for disk storage.

MEETING INSATIABLE STORAGE REQUIREMENTS

If there is one thing developers cannot get enough of, it is storage.

NAND flash steals most of the limelight when it comes to storage. It is available in a mind-boggling array of form factors, capacities, and performance characteristics. The spread includes SLC (single layer cell), MLC (multi-layer cell), and TLC (triple layer cell) that trade off capacity for performance and reliability. In larger systems, various types of flash memory exist in a storage hierarchy (see "Flash Software Rules in Hierarchical Storage" on [electronicdesign.com](#)).

At the base of the hierarchy is Diablo Technologies' Memory Channel Storage (MCS) architecture, which puts flash right next to the microprocessor in DIMM slots with products like SanDisk's UltraDIMM (Fig. 1). NVMe flash storage on the PCI Express bus is the next level up, with solid-state disks above that.

Flash will also be on the cutting edge of 3D silicon technology with multi-layer 3D NAND chips [see "Mass Production Underway for 32-Layer 3D V-NAND Flash" on [electronicdesign.com](#)]. These address the push for higher densities and performance.

Flash storage alternatives like FRAM and MRAM continue to grow, although they are still addressing niche markets. STT-MRAM (spin-transfer torque) prototypes were shown in 2014, and currently available MRAM has seen growth in demand and capacity (see "Q&A: Everspin Takes MRAM to the Mainstream" on [electronicdesign.com](#)). Conductive bridging RAM is on the horizon this year, as well (see "Conductive Bridging RAM" on [electronicdesign.com](#)).

FRAM is starting to replace flash completely in microcontrollers like Texas Instruments' MSP 430 (see "Low Power Microcontroller Has Up to 128 Kbytes of FRAM" on [electronicdesign.com](#)). The MSP430FR6xx (Fig. 2) has 128 Kbytes of FRAM and 2 Kbytes of SRAM.

Embedded MMC (eMMC) flash will continue to deliver in the embedded and mobile space. Capacities will be up as well as throughput. Much of this push is due to things like 4K video capture support found in high-end smartphones.

There is also the bursty nature of these applications, including IoT applications where fast flash storage is needed, but long term storage needs higher capacities. Hybrid flash with chameleon-like properties will bring the speed of SLC with the capacity of MLC and TLC, allowing designers to arbitrarily choose the boundary between the two based on application requirements.

DDR4 is starting to reach full stride. DIMMs are available in a wide array of configurations and it is the interface found on all high-performance processors and motherboards. Intel's Haswell supports DDR4 and the forthcoming Intel Skylake architecture will support DDR3 and DDR4.

DDR4's premium price is dropping and its advantages over DDR3 are significant. It uses 20% less power and can run at 1.2 V. Performance tops out around 3200 MHz, although 4000 MHz could be available in the future. Enterprise solutions will push the capacity per DIMM as high as possible.

This year we may see new high-performance systems that utilize technologies like the Hybrid Memory Cube (see Hybrid Memory Cube Shows New Direction for High-Performance Storage on [electronicdesign.com](#)). This is also a 3D silicon technology, but targeting DRAM.

FASTER, USING LESS POWER, AND MORE SECURE

Have no fear: 8- and 16-bit micros have not gone away. They will continue to be challenged by 32-bit solutions, primarily built around the ARM Cortex-M0+ architecture, that continue to push down into the low power space. At this point, vendors with a mix of 8-, 16-, and 32-bit micros have unified their I/O structure and development tools simplifying migration, although most developers tend to stick with one platform.

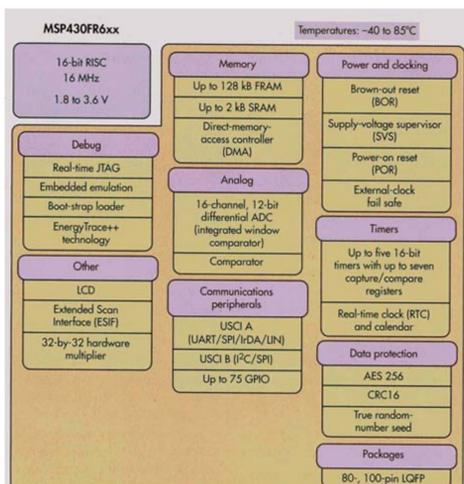
IoT is one reason for the push to 32 bits, and a lot of that has to do with communication and security. Communication stacks can benefit from the wide word size and addressing capability. Security is more than some crypto instructions and a random number generator (RNG). These are necessary, but features like secure boot and storage tend to be part of the mix these days. The challenge for developers is that homes and sites may have hundreds of IoT devices, thereby greatly increasing the attack surface. Making these devices more secure helps mitigate the threat.

Intel's Broadwell-K and Skylake platforms are due in mid-2015. Skylake is the "tock" in Intel's tick-tock release cycle that refines the Broadwell architecture with improved performance and reduced power requirements. Intel has announced its synthesizable Atom core that should be seeing more traction in 2015 with partners like Rockchip. Mobile solutions will begin the transition from 22-nm to 14-nm.

ARM partners continue to challenge Intel across the board from the 64-bit ARMv8 Cortex-A50 series, which will finally see major shipments this year through the mid- and low-end space where ARM has been dominant. The announcement of the Cortex-M7 (see "Cortex-M7 Takes Aim at the IoT High Ground" on [electronicdesign.com](#)) in 2014 pushes the microcontroller solution into the Cortex-A space in terms of performance, challenging many proprietary digital signal controller (DSC) architectures.

Cortex-A53 and Cortex-A57 will be showing up in everything from high-end smartphones and tablets to cloud and communication servers. Cavium's ThunderX family now packs 48 ARMv8 cores into a single CN88xx chip.

Virtualization will continue to make inroads in deeply embedded. It provides a way to integrate legacy systems onto a single platform as well as providing isolation for functionality and security reasons. Virtualization already dominates in the cloud and the enterprise, where network function virtualization (NFV) is bringing networking closer to the applications.



2. MSP430FR6XX has 128 Kbytes of FRAM and 2 Kbytes of SRAM. SRAM still has a performance edge, but FRAM is used for code and data storage.



3. Avnet's PicoZed is a compact system-on-module (SOM) that holds a Xilinx Zynq FPGA with dual Cortex-A9 cores.

FPGAs AND HIGH-PERFORMANCE CHALLENGES

Hard or soft cores in an FPGA are the norm these days. Soft cores are even suitable for many of the low-power, flash-based FPGAs that provide the flexibility of an FPGA with the functionality of a microcontroller, with fewer product lifetime issues.

Modules like Avnet's PicoZed (Fig. 3) system-on-module (SOM) and Digilent's Zybo (see "Hard-Core FGPA Provides A Flexible Development Target" on [electronicdesign.com](#)) are providing compact delivery and development support for Xilinx's Zynq-7000 FPGA, with dual Cortex-A9 cores capable of running operating systems like Linux. Hard-core processors allow more flexible communication support for an FPGA solution. Altera's 14-nm Stratix 10 can include a four-pack of ARM Cortex-A53 cores.

Translating OpenCL design to FPGAs moves from the lab to the mainstream. Altera and Xilinx provide OpenCL support as alternatives to their conventional FPGA design tools. FPGAs can also be incorporated into a server using Intel's QuickPath Interconnect (QPI), but this is only one approach available to users looking for higher performance.

GPUs are commonly found in supercomputers and racks where high-performance computing is needed. This year adds more power-efficient cores to the mix. Intel Knights Landing Xeon's Phi continue the use of lots and lots of x86 cores designed to work with Intel's Silicon Photonics optical interconnect.

Keep an eye out for some of the new compute platforms from massively parallel CPUs to Microns Automata Processor (see "Making a New Type of Parallel Processing Possible" on [electronicdesign.com](#)). Parallel processing is cropping up in in unexpected places.

FPGA prototyping will be key to shortening ASIC development times as EDA vendors deliver improved verification productivity and early software bring-up. All levels of simulation continue to be very important as the cost of generating silicon rises. The challenge will be the transition between these levels.

Increasing functional consolidation into a single SoC is pushing ultra-large designs. Mary Ann White, director of product marketing, Galaxy Design Platform for Synopsys, notes, "While 16- and 14-nm FinFET technologies become a reality by moving into production for high-performance applications, the popularity of the 28-nm node will persevere, especially for mobile and IoT (Internet of Things) devices." A significant number of designs are approaching 1 billion transistors.

CONNECTIVITY FOR IoT

Wired and wireless connectivity is the hallmark of IoT devices. Devices will have one or more connections such as the latest Bluetooth 4.2 or USB 3.

Bluetooth 4.2 will be the target for integrated designs. It provides faster throughput, IPv6 support, and improved privacy. For example, a smartphone implementation could allow selective connections to local beacons based on user preferences.

USB 3 adoption will be helped by the new Type-C connector (see "USB 3.1 Type C Connector Is Reversible" on [electronicdesign.com](#)). The reversible design is akin to the style used with Apple products like the iPhone.

Adoption of USB's advanced power management is on the rise. USB has long since stepped past the 2.5 W for the USB 2.0 standard. USB 3 systems can deliver up to 100 W at 20 V.

PCI Express (PCIe) Gen 3 remains the primary high-speed interconnect. An x16 configuration can support 40 Gbit/s Ethernet, but 100 Gbit/s Ethernet is on the map along with software defined networking (SDN). SDN switch chips like Cavium's XPliant and Broadcom's StrataXGS Tomahawk Series (see "Chips Make Software Defined Networking Work" on [electronicdesign.com](#)) were announced in 2014. They will provide a flexible platform for 100 Gbit/s Ethernet as well as various combinations of lower-speed Ethernet incarnations.

Gigabit Ethernet is common now, but 2.5 Gbit/s Ethernet and even 5 Gbit/s Ethernet may be on the horizon for device connections. These speeds also lead to higher-end links like 25 Gbit/s Ethernet.

Many of the new multicore chips are designed for the 40 Gbit/s and 100 Gbit/s Ethernet space. They are designed to support NFV with connections to SDN switches to create a software configurable environment. This approach is turning from theory into the norm in 2015.

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